What is Claimed is:

[c1] A content addressable memory (CAM) having first and second SRAMs with P-channel PFET passgates for storing first and second memory bits, and a compare logic circuit, with the CAM providing a full array search with the ability of per bit masking.

[c2] The CAM cell of claim 1, having a reverse beta ratio of substantially 2, which is the reciprocal of the beta ratio which is the ratio of conductivity of a pull down device to the conductivity of a passgate device of a SRAM cell, to allow READ and WRITE operations at first and second ports of the CAM with conventional support circuitry.

[c3] 3. The CAM cell of claim 1, comprised of 8 PFET devices and 8 NFET devices.

[c4] The CAM cell of claim 1, wherein each of the first and second SRAMs comprises 6 devices, 2 NFET pull down devices, 2 PFET pull up devices, and 2 PFET passgate devices, a passgate left device and a passgate right device.

[c5] The CAM cell of claim 4, where the compare logic circuit comprises an XOR gate comprising 4 NFET devices.

[c6] The CAM cell of claim 4, including 2 wordlines, WLA for the first SRAM and WLB for the second SRAM, 2 bitlines, bitline left BL and bitline right BR, 2 searchlines, searchline left SL and searchline right SR, and a matchline ML.

[c7] The CAM cell of claim 6, wherein the CAM cell shares search bitlines and read/write bitlines, and unselected bitlines are held at ground to allow disabling of the compare logic circuit during SRAM read/write operations.

[c8] The CAM cell of claim 7, wherein each bitline standby bias is Â½ VDD.

[c9] The CAM cell of claim 4, wherein the lay out of the 6 devices of the second SRAM is reversed in the circuit layout with respect to the lay out of the 6 devices of the first SRAM.

[c10] The CAM cell of claim 5, wherein the 6 devices of the first SRAM are formed at intersections of first and second active silicon regions with first, second and

third polysilicon conductors, the 6 devices of the second SRAM are formed at intersections of second and third active silicon regions with fourth, fifth and sixth polysilicon conductors, the 4 devices of the XOR gate are formed at intersections of the second active silicon region with third, sixth, seventh and eight polysilicon conductors.

[c11] The CAM cell of claim 10, wherein the 6 devices of the second SRAM are laid out symmetrically opposite to the 6 devices of the first SRAM with an inverted, relative to the first active silicon region, third active silicon region, and an inverted, relative to the first polysilicon conductor, fourth polysilicon conductor, and inverted, relative to the second and third polysilicon conductors, fifth and sixth polysilicon conductors.